CLAIMS

1. A method for managing control structure access, said method comprising

configuring a memory window manager to communicate with a processor and a plurality of control structures, wherein data is communicable between said processor and said plurality of control structures; and

automatically specifying which control structure among said plurality of control structures is accessible by said processor utilizing said memory window manager.

2. The method of claim 1 wherein said memory window manager specifies which control structure among said plurality of control structures is mapped into an address space of said processor.

3. The method of claim 1 further comprising:

arranging said memory window manager to comprise at least four elements, which can be mapped into said address space of said processor.

4. The method of claim 3 wherein at least one element of said at least four elements comprises an element which permits said processor to program a base address in a memory for control structure storage.

5. The method of claim 3 wherein at least one element of said at least four elements comprises an element that allows said processor to specify a size for each control structure among said plurality of control structures.

6. The method of claim 3 wherein at least one element of said at least four elements permits said processor to specify an index number associated with a control structure among said plurality of control structures that is desired to be accessed by said processor.

7. The method of claim 3 wherein at least one element among said at least four elements comprises a memory window that permits said processor to access a control structure among said plurality of control structures based on a index number associated with said control structure.

8. The method of claim 1 wherein said processor comprises a Central Processing Unit (CPU) of a computer.

9. The method of claim 1 further comprising:

configuring said memory window manager to comprise an address computation engine.

10. A system for managing control structure access, said system comprising

a processor which communicates with a plurality of control structures thereof;

a memory window manager which communicates with said processor and said plurality of control structures, wherein said memory window manager specifies which control structure among said plurality of control structures is accessible by said processor.

11. The system of claim 10 wherein said memory window manager specifies which control structure among said plurality of control structures is mapped into

an address space of said processor.

12. The system of claim 10 wherein said memory window manager comprises at least four elements, which can be mapped into said address space of said processor.

13. The system of claim 12 wherein at least one element of said at least four elements comprises an element which permits said processor to program a base address in a memory for control structure storage.

14. The system of claim 12 wherein at least one element of said at least four elements comprises an element that allows said processor to specify a size for each control structure among said plurality of control structures.

15. The system of claim 12 wherein at least one element of said at least four elements permits said processor to specify an index number associated with a control structure among said plurality of control structures that is desired to be accessed by said processor.

16. The system of claim 12 wherein at least one element among said at least four elements comprises a memory window that permits said processor to access a control structure among said plurality of control structures based on a index number associated with said control structure.

17. The system of claim 10 wherein said processor comprises a Central Processing Unit (CPU) of a computer.

18. The system of claim 10 wherein said memory window manager comprises:

a memory window manager module located in a memory location of a computer, wherein said memory window manager module communicates with said processor and said plurality of control structures, wherein said memory window manager module specifies which control structure among said plurality of control structures is accessible by said processor.

19. The system of claim 10 wherein said memory window manager comprises an address computation engine.

20. A system for managing control structure access by a Central Processing Unite (CPU), said system comprising

a CPU of a computer, wherein said CPU communicates with a plurality of control structures thereof;

a memory window manager module which communicates with said CPU and said plurality of control structures, wherein said memory window manager module specifies which control structure among said plurality of control structures is accessible by said CPU and wherein said memory window manager module further specifies which control structure among said plurality of control structures is mapped into an address space of said CPU;

wherein said memory window manager comprises at least four elements, which can be mapped into said address space of said CPU, including:

a first element of said at least four elements that permits said CPU to program a base address in a memory for control structure storage.

a second element that allows said CPU to specify a size for each control structure among said plurality of control structures.

a third element that permits said processor to specify an index number associated with a control structure among said plurality of control structures that is desired to be accessed by said processor;

a fourth element comprising a memory window that permits said processor to access a control structure among said plurality of control structures based on an index number of a control structure among said plurality of control structures.